Model 2249W
12-Channel ADC with Wide Gate

Analog Inputs: Twelve; Lemo-type connectors; charge-sensitive (current-integrating); AC-coupled (2 msec time constant, field changeable); 50 Ω impedance; linear range normally 0 to -2.0 V; protected to ±50 V against 1 μsec transients.
Gain: -0.25 pC/count ±5%.
Full Scale Range: Approximately -500 pC (maximum count ≅ 1980).
Integral Non-linearity: ±0.05% ±(0.5 pC +0.1%).
ADC Resolution: A 5 V, 20 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 0.5 pC (2 counts).
Gate Input: One gate common to all ADCs; Lemo-type connectors; 50 Ω impedance; -600 mV or greater enables; minimum duration, 30 nsec; maximum recommended duration up to 10 μsec; partial analog input must occur within 0.5 μsec after opening gate to preserve accuracy, effective opening and closing times; 5 nsec; internal delay, 7 nsec.
Fast Clear: One front-panel input common to all ADCs; Lemo-type connector; 50 Ω impedance; -600 mV or greater clears, minimum duration, 50 nsec. Requires additional 2.0 μsec settling time after clear.
Pedestal: Adjustable over approximately 100 counts via side-panel accessed trimmer capacitor. Somewhat higher for wide gate.
Test Function: With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to +12 V) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of -15 pC/V into all inputs at F(25) • S2 time. (With CAMAC I not present F(25) • S2 will generate the gate only, providing a measure of residual pedestal.)
Digitizing Time: 106 μsec.
Q and LAM Suppression: Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging: CAMAC #1 module.
Current Requirements: +24 V at 143 mA; -24 V at 75 mA; +6 V at 725 mA; -6 V at 155 mA.

Model 2259B
12-Channel, Peak-Sensing ADC

Analog Inputs: Twelve; Lemo-type connectors; voltage (peak) sensing; direct-coupled, quiescently at approximately +0.5 mV; 50 Ω impedance; protected to ±100 V against 1 μsec transients; accepts either negative-going pulses of ≥ 50 nsec rise time or bipolar pulses with negative lobe first.
Gain: (1 ±0.05) counts/mV.
Full Scale Uniformity: ±5%.
Integral Linearity: ±(0.1% + 1 count) from 7% to 100% of full scale.
ADC Full Scale: 2020 ±20 counts.
Long-Term Stability: Better than 0.25% of reading ±4 mV/week (at constant temperature).
Temperature Coefficient: Typical, 0; maximum, ±0.03%/°C of full scale.
ADC Isolation: A -5 V, 100 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 5 mV.
Gate Input: One gate common to all ADCs; Lemo-type connectors; 50 Ω impedance; -600 mV or greater enables; minimum duration, 100 nsec; maximum recommended duration, 5 μsec; effective opening and closing times; 2 nsec; internal delay, 5 nsec; must enclose negative peak of input pulse; pulse position dependence within the gate < 2 counts/μsec.
Fast Clear: One front-panel input common to all ADCs; Lemo-type connector; 50 Ω impedance; -600 mV or greater clears, minimum duration, 50 nsec. (Caution: narrower pulses cause partial clearing.) Requires additional 2 μsec settling time after clear.
Pedestal: 35 ±25 counts with dependence on gate width < 2 counts/μsec.
Test Function: With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to ≈10 V) or optional rear connector P1, P2, or P5 patch points will inject signal with a proportionality constant of -0.167 V/V into all inputs at F(25) • S2 time. (With CAMAC I not present F(25) • S2 will generate the 100 nsec gate only, providing a measure of residual pedestal only.)
Digitizing Time: 106 μsec.
Q and LAM Suppression: Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 200) before data is considered useful. A module in which all channels contain less than set amount will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging: CAMAC #1 module.
Current Requirements: +24 V at 35 mA; -24 V at 15 mA; +6 V at 850 mA; -6 V at 200 mA.